Abstract: As the increasing penetration of modular multilevel converter (MMC)-based high-voltage direct current (HVDC) into bulky power transmission systems, the performance of MMC on dealing with DC faults, especially on temporary DC fault in overhead transmission lines, has been more and more significant. A comprehensive overview of MMC on DC fault ride-through (FRT) capability is discussed. Compared with DC fault blocking capability considered as a passive DC FRT strategy focusing on isolating DC fault from AC sides, the DC FRT capability emphasises remaining converters continuous operating during DC faults to regulate and support the connected AC grids. The principle and prerequisite of MMC on DC FRT are analysed, and then improved MMC topologies with DC fault handling capability are summarised and a corresponding comparison among them is conducted. Finally, applications of MMC with DC FRT capability on HVDC systems and its relative control strategies are presented.

1 Introduction

High-voltage direct current (HVDC) transmission systems based on voltage source converter (VSC), as a potential solution for large-scale power transmission and renewable energy integration, have attracted many attentions [1–8]. Of the many technique challenges, operation and protection during DC fault that occur more frequently in overhead transmission applications has become a main barrier for the development of HVDC systems, especially multi-terminal DC systems. In contrast to the traditional two-level VSCs which contain a single large central DC capacitor that can cause severe discharging current under a DC fault, modular multilevel converters (MMCs) avoid such issue due to its configuration of large numbers of small distributed DC capacitors connected in the DC-link of each sub-modules (SMs). MMC also has many other advantages such as modular design, high efficiency and scalability, excellent output waveform with low harmonic distortion etc. [9–17].

The basic building block in an MMC is an SM. The half-bridge SM (HBSM) as shown in Fig. 1a has been the main configuration in the MMC. However, HBSM-based MMC (HB-MMC) does not have DC fault handling capability and, thus, has to rely on AC or DC circuit breakers (CBs) to isolate DC faults [18, 19]. This becomes problematic for both converters since it has to withstand high fault current from the connected network, as a result it could take considerable time for the system (especially a multi-terminal system) to recover from such a DC fault. Using DC CB (DCCB) is a quick and efficient method to isolate the DC fault, especially for the multi-terminal HVDC systems. However, unlike AC systems, no zero crossing in the DC current makes it difficult to open the DCCB. Though the DCCB has recently been developed, the technique is not mature and highly cost-consuming [20, 21].

To improve the performance of MMC under DC fault conditions for HVDC systems, extensive research on improved MMC topologies and enhanced control strategies with DC fault ride-through (FRT) capability have been conducted in recently published papers [22–64]. According to the response features of the converter, the DC FRT capability can be divided into two categories: passive DC FRT strategy and active DC FRT strategy. The passive DC FRT strategy, also named as DC fault blocking capability is to control the MMC working on blocking status with all insulated gate bipolar transistors (IGBTs) switching off. Though the fault current can be forced to zero and DC fault can be isolated from AC side, the converter loses the control of electrical quantities on AC side such as AC voltage, AC current, active and reactive powers, which as a result will severely affect the connected AC grid, especially in a weak AC grid. An active FRT scheme was proposed to deal with this issue. After DC fault happens, the MMC with active FRT capability can not only isolate the DC fault, but also continue operating and regulating the connected AC grid during the fault period. Such advantages can provide significant benefits for HVDC systems with overhead transmission lines, as it is more frequent for HVDC system with overhead lines than that with cable lines, to have temporary DC faults caused by lightning strikes or mechanical faults caused by broken branches or bushes, which however can normally be cleared quickly [49].

This paper summarises the most recent developments on DC FRT capability of MMC for HVDC systems, covering improved MMC topologies and enhanced operation strategies. It is organised as follows: Section 2 introduces the basic operation and traditional DC fault behaviour of HB-MMC. The principle of DC FRT strategy is summarised in Section 3, and various improved topologies with DC FRT capability are presented and discussed in Section 4. Furthermore, Section 5 introduces utilisations of MMC with active DC FRT capability on HVDC systems, and finally some conclusions are shown in Section 6.

2 Basic operation and DC fault behaviours

2.1 Basic MMC operation

Fig. 1a shows the structure of one phase of an MMC, which is composed of either of two classic SMs, i.e. HBSM as shown in Fig. 1b or full-bridge SM (FBSM) as shown in Fig. 1c. \( V_{dc} \) is the DC-link voltage, \( L_a \) is the arm inductor in each arm and \( C \) is the capacitor in each SM. \( v_{pa} \) and \( v_{na} \) are the total voltages generated by all the SMs in the upper and lower arms, respectively. \( i_{pa} \) and \( i_{na} \) are the current in the upper and lower arms, respectively. \( i_a \) is the output AC phase current. Under normal operation conditions, FBSM-based MMC (FB-MMC) is typically controlled as same as the HBSM-based.

According to Fig. 1a, the arm currents \( i_{pa} \) and \( i_{na} \) can be expressed as...
Equivalent circuit of HB-MMC under blocking mode

Basic structure of an MMC and two different classic SMs

According to [11], the output phase voltage and the circulating current in phase a flowing through both the upper and lower arms and has no effect on the output phase current. According to [11], the output phase voltage and the circulating current of the MMC are given as

\[ i_{pa} = \frac{i_a}{2} + i_{cm\omega} \]  \hspace{1cm} (1)

\[ i_{ma} = -\frac{i_a}{2} + i_{cm\omega} \] \hspace{1cm} (2)

where \(i_{cm\omega}\) is the common-mode current in phase \(a\) flowing through both the upper and lower arms and has no effect on the output phase current.

Thus, the operation principle of MMC aims at controlling the upper and lower arm voltages to regulate the AC side and the DC side voltages.

2.2 DC fault behaviours of HB-MMC under IGBTs blocking mode

To analyse the behaviours of conventional HB-MMC during DC fault, two stages were considered [65, 66]. On Stage 1, the MMC is not blocked, the DC cable capacitor and some of the capacitors within the SMs whose \(S1\) is ON (named as switched-in SM capacitors, see Fig. 1b) will discharge. As this stage is very short, fault current from the AC grid is insignificant due to the relatively large transformer leakage impedance, and thus the fault current on the converter arm and DC side is primary due to the DC capacitor discharging. After the fault is detected by over-current on the converter arm and DC side, the MMC is blocked. The system then moves to Stage 2. The simplified circuit during Stage 2 is shown in Fig. 2 where the serial-connected diodes (in the example as shown in Fig. 1b, \(D2\)) continue feeding AC fault current into DC side.

On the basis of the above analysis, it is found that the arm fault current mainly includes two components: AC feeding-in fault current and SM capacitors discharging current. Though capacitors discharging current damps to zero after IGBTs blocking, the AC fault current continues feeding into the converter due to the anti-parallel diodes in IGBTs, the converter thus cannot isolate the DC fault. The traditional scheme is to physically disconnect the converter from the AC grid by switching off AC CBs (ACCBs) at the AC side, as shown in Fig. 2. However, as the aforementioned, the converters have to withstand high fault current from the connected network since it could take considerable time for the system (especially a multi-terminal system) to recover from such a DC fault, due to the inherent slow mechanical response of the ACCBs.

3 Principle of DC FRT strategy

On the basis of the above analysis, to achieve the DC FRT, the primary task is to make the AC feeding-in fault current controllable. The traditional scheme with ACCB is lack of dynamic response performance under fault conditions. Recently, several improved MMC topologies by adding extra power semiconductors were proposed to enhance the DC FRT capability. According to the effect on AC feeding-in fault current, the ride-through strategies can be divided into two groups such as passive DC FRT also known as DC fault blocking capability [22–24, 26, 27, 31, 32, 34–36, 39–41, 47, 48, 56, 57, 59] and active DC FRT capability [25, 28–30, 33, 37, 38, 42–46, 49–55, 60–64].

3.1 Principle of passive DC FRT

The purpose of passive DC FRT capability is to passively eliminate the AC feeding-in current to zero. To achieve this object, two types of strategies were proposed: the first scheme is offering the other
lower-impedence path for the AC feeding-in current by making AC side short-circuited, so as to eliminate the AC current flowing through the converter to the DC side, though the AC side current is not equal to zero. The equivalent circuit is shown in Fig. 3a. The other scheme is using the series capacitors in the arm to generate an opposite voltage polarity, which can be typically achieved by FB-MMC, to the direction of the AC feeding-in fault current so as to force it to zero, as shown in Fig. 3b.

3.2 Principle of active DC FRT

Though the fault current can be forced to zero and DC fault can be isolated from AC side by using the passive DC FRT strategy, the AC circuit would be short-circuited or the converter would be isolated from AC side by using the passive DC FRT strategy, the AC network would lose the control of electrical quantities on AC side such as AC voltage, current, instantaneous active and reactive powers which will severely affect the connected AC grid, especially in a weak AC grid. To solve this issue, the active ride-through strategy was proposed, where the objective is not only to isolate the DC fault, but also to continue operating and regulating the connected AC grid during the fault period. The equivalent circuit is shown in Fig. 4.

Assuming the DC voltage under fault conditions is $V_{\text{dc}}$, the operation characteristics of MMC on the AC and DC sides can be rewritten as

\[
\begin{align*}
\epsilon_a &= \frac{v_{na} - v_{pa}}{2} \\
v_{\text{dc}}' &= v_{pa} + v_{na}
\end{align*}
\]

Thus, the required arm voltage generated by SMs can be expressed as

\[
\begin{align*}
v_{pa} &= \frac{v_{\text{dc}}'}{2} - \epsilon_a \\
v_{na} &= \frac{v_{\text{dc}}'}{2} + \epsilon_a
\end{align*}
\]

According to the aforementioned analysis in Section 2.1, the current $i_s$ is controlled by regulating the $\epsilon_a$, so $\epsilon_a$ generated by the MMC should match the requirement of AC current reference. Additionally, under the DC fault conditions, $v_{\text{dc}}'$ is lower than the normal value $V_{\text{dc}}$, even equal to zero under zero-voltage DC fault. Thus, the prerequisite of active DC FRT capability for the MMC is to produce enough negative arm voltages by the SMs to defend the AC side voltage.

4 Improved MMC topologies with DC FRT capability

The common method to generate negative voltage output in the MMC is using the full-bridge-based SM (i.e. $S_2$ and $S_3$ switches on as shown in Fig. 1c), and the FB-MMC is an acknowledged topology which has the inherent advantage of DC FRT capability [49, 53–55]. By using the negative voltage state of the FBSMs, the SMs can generate negative arm voltage, which make the operation of FB-MMC independent to the DC voltage. As a result, the HVDC based on FB-MMC can be flexibly operated at a reduced DC voltage, even zero DC voltage, under adverse weather conditions and high degree of pollution in the area of the overhead lines. However, FB-MMC is not an ideal solution on the DC fault, due to the double number of SM power devices compared with the HBSM. This not only increases the costs of high-power MMC systems, but also results in higher-power loss as the current in each SM flows thought two power devices instead of one as in an HBSM. Recently, several improved topologies are proposed to enhance the performance of MMC on handling DC fault including both passive and active DC FRT strategies.

4.1 Parallel-connected thyristor

To protect the freewheeling diode in the IGBT during DC faults, a single thyristor (ST) is usually parallel connected to the AC terminal of the SM to share the fault current with freewheeling diode, as shown in Fig. 5a [24]. By switching the thyristors on after a DC fault detecting, most of the fault current would flow through the thyristors rather than the diodes. However, this method can only protect the semiconductor devices, but not prevent the AC fault current feeding into the DC side. A solution for this drawback was introduced later by employing a double thyristors (DTs across SM), as shown in Fig. 5b [22]. On the basis of this scheme, the freewheeling effect of diodes is eliminated and the DC fault current is allowed to freely decay to zero. The shortcoming of this method is increasing the device complexity due to embedding DTs in each SM. An alternative scheme by combining and connecting the DTs across the AC output terminal of the converter (DT across AC side) was proposed in [23], as shown in Fig. 5c. Though the parallel-connected thyristor can segregate the AC side from the DC side, the AC side of the converter is uncontrolled and short-circuited when the thyristors switch on. Thus, this scheme has passive DC FRT capability instead of active ride-through capability.

4.2 Hybrid SM-based MMC topologies

4.2.1 HBSM plus HBSM: A clamp-double SM (CDSM) circuit was proposed including two serial HBSMs plus one IGBT and two diodes, as shown in Fig. 6a [31, 32, 57, 58]. In normal operation, the CDSM is equivalent to two serial HBSMs, as $S_1$ is always closed. So the total losses are slightly increased. In case of a DC fault, $S_1$ is turned off, then the fault current has two parallel paths to flow through half capacitors in each arm, which can offer enough reverse voltage to push the fault current to zero. As a result, this scheme has DC fault blocking capability, which is
passive DC FRT. In [58], a static synchronous compensator (STATCOM) operation scheme for the CDSM-based MMC (CDSM-MMC) during a pole-to-pole DC fault was proposed. By using the output negative voltage state of CDSM when the arm current flowing through it is negative, the arms of the CDSM-MMC can operate in the conducting mode and blocked mode alternately. With the proposed control strategy, the CDSM-MMC is capable of keeping the reactive power control and the capacitor voltage balanced during the DC fault. However, by using this control strategy, the AC current would deprived active FRT capability. When a DC fault is detected, all switching devices are then blocked and the fault current flows through all capacitors in the SMs, as shown in Fig. 8b. Similarly, for the hybrid MMC topology with half HBSMs and half FBMSs as shown in Fig. 7a, if the FBSM does not need to generate the negative voltage state, S3 could be permanently off and therefore can be removed. However, the diode is still required to provide a path for the fault current during a DC fault. Thus, the simplified circuit still has DC fault blocking capability, but deprives active FRT capability. When a DC fault is detected, all switching devices are then blocked and the fault current flows through all capacitors in the SMs, as shown in Fig. 8a.

On the basis of the simplified FBSM without S3, two other different hybrid MMC topologies are derived [27, 35]. A hybrid MMC consisting of HBSMs and simplified FBSMs was presented, and the relative reliability and redundancy of this structure were analysed in [27]. In [35], two simplified FBSMs were combined as a modified three-level cell, as shown in Fig. 8c, and then a hybrid MMC including HBSMs and modified three-level cells was proposed.

From the above analysis, it can be summarised that the motivation of simplified SM circuit is to remove some power semiconductors (usually IGBT in FBSM) to reduce the device cost, but with a sacrifice of the lack of generating negative voltage in the arm voltage. Thus, all above-mentioned hybrid MMC topologies...
with simplified SM circuits only have DC fault blocking capability rather than active DC FRT capability.

4.2.4 Hybrid cascaded MMC topology: As shown in Fig. 9 [42, 64], HBSMs in the main power stage are used to generate the fundamental output voltage lower switching frequency and the cascaded FBSMs which are serially connected to its AC terminals are used to attenuate the output voltage harmonics. Derived from the hybrid multilevel converter which is consisted of the two-level converter in series with cascaded FBSMs [60–63], the hybrid cascaded MMC topology avoids the shortcomings of the two-level converter in the main power stage in terms of high-power semiconductor voltage stresses, single central DC capacitor and output voltage harmonics. Since the cascaded FBSMs at the AC terminal can not only offer enough voltage to reverse the AC voltage, but also regulate the AC current during the fault, so this topology also has the active DC FRT capability. One disadvantage of this structure is relatively higher-power losses, especially the conduction losses in the cascaded FBSMs, since all transmission powers would flow through the cascaded FBSMs at the AC terminal.

4.2.5 Alternate arm converter: Alternate arm converter (AAC) is considered as a hybrid topology between MMCs due to the presence of FBSMs and the two-level converter, in form of director switches in each arm [43–46]. As shown in Fig. 10, each arm of the converter consists of a stack of FBSMs, a director switch and an arm inductor. The operation feature of this topology is to employ one arm per half cycle to produce the AC voltage, that is, by using the upper arm to generate the positive half cycle of the AC sine wave and the lower arm for the negative part. With the ability of its arm to produce negative voltage, the AAC can continue operating when DC voltage collapses. Thus, this structure has the active DC FRT capability. However, its main drawback is the director switches are exposed to high inrush currents during current commutation between the upper and lower arms [60].

4.3 Modified HBSM topologies

Several different modified HBSM topologies were proposed in [47, 48], by adding extra IGBTs or diodes to eliminate the freewheeling effect of anti-parallel diode. In [48], a diode clamp SM circuit was
presented by adding an extra IGBT and two diodes, as shown in Fig. 11a. In normal operation, S1 is always switched on, D4 is kept in off-state, the arm current flows through S3 and D3, the SM is equivalent to a conventional HBSM. In case of DC fault, all IGBTs are switched off, the fault current flows through half capacitors in the arm, as shown in Fig. 11a. Two other simpler schemes were presented in [47], in which one extra IGBT and diode was serially connected to S2 (as shown in Fig. 11b) or three more diodes were added in each SM (as shown in Fig. 11c). These two methods are using reverse-connected diodes to isolate the fault current flowing through AC side to DC side, after all IGBTs blocking in case of DC fault. The above-mentioned methods eliminate the freewheeling effect of anti-parallel diode in the conventional HBSM; as a result, the converters with these topologies obtain the DC fault blocking capability.

4.4 Comparisons

A comparison among the improved MMC topologies with DC FRT capability is carried out, in terms of the extra number of power semiconductors (assuming N SM in each arm) and DC FRT capability, as listed in Table 1. It can be found that there are three types of topologies with the active DC FRT capability, and the additional semiconductors compared with HB-MMC in each arm are almost equal, that means, the principle of these three types of topologies is to replace half HBSMs with FBSMs in each arm so as to produce enough negative arm voltages by the SMs to defend the AC side voltage, as the above analysis in Section 3.2.

5 Active DC FRT strategy in MMC-based HVDC systems

As the increasing development and implementation of HVDC systems, operation and protection during DC faults that occur more frequently in overhead transmission applications has become one of the most significant challenges for the development of HVDC systems, especially multi-terminal DC systems.

The traditional DC FRT strategies are concerned about fault isolation or clearance. For the conventional MMC without DC fault handling capability, the ACCBs or DCCBs are required to isolate the converter from AC or DC grids. Owing to the inherent slow mechanical response of the ACCBs, the converters have to withstand high fault current from the connected network since it could take considerable time for the system (especially a multi-terminal system) to recover from such a DC fault. Using DCCB as an alternative method to physically disconnect the converter from the DC fault. It is mainly categorised into three groups such as mechanical, solid-state and hybrid DCCBs. Though the classical mechanical DCCB exhibit excellent performance on power losses, the reaction time is still long due to the need for eliminating the arc [67]. The solid-state DCCB is able to offer fast response in few microseconds, but with the sacrifice of higher-power losses and device costs. To combine the features of mechanical DCCB and solid-state DCCB, the hybrid DCCB was proposed including a mechanical path as the normal conduction path with lower on-state power losses and a parallel-connected solid-state breaker providing fault circuit interruption [68]. However, the hybrid DCCB still has relatively large dimensions and high device costs.

An alternative scheme adopting DC/DC transformers based on power electronic devices was proposed for HVDC grid interconnections. Since the DC/DC transformer has the features of power flow control, DC voltage transform and DC fault blocking, it can be used to isolate the faulty DC grid section so as to achieve the DC FRT function.

<table>
<thead>
<tr>
<th>Types</th>
<th>Extra semiconductors compared with HB-MMC (per arm)</th>
<th>DC FRT capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>parallel-connected thyristor</td>
<td>ST [23] N thyristors + 2N diodes</td>
<td>passive</td>
</tr>
<tr>
<td>HBSM</td>
<td>DT across SM [23]</td>
<td>passive</td>
</tr>
<tr>
<td>FBSM+</td>
<td>DT across AC side [22]</td>
<td>passive</td>
</tr>
<tr>
<td>hybrid SM</td>
<td>CDSM [30] 0.5N IGBTs+N diodes</td>
<td>passive</td>
</tr>
<tr>
<td></td>
<td>CCSM [36] N IGBTs+N diodes</td>
<td>active</td>
</tr>
<tr>
<td></td>
<td>FBSM+ 1:1 HBSM [24]</td>
<td>active</td>
</tr>
<tr>
<td></td>
<td>2:1 1.33N IGBTs+</td>
<td>active</td>
</tr>
<tr>
<td>simplified SM</td>
<td>CDSM [25] 0.5N IGBTs+N diodes</td>
<td>passive</td>
</tr>
<tr>
<td></td>
<td>1:1 0.44 IGBTs+</td>
<td>passive</td>
</tr>
<tr>
<td>hybrid cascade</td>
<td>two-level [34] 0.88N diodes</td>
<td>passive</td>
</tr>
<tr>
<td>AAC [42]</td>
<td>N IGBTs+N diodes</td>
<td>active</td>
</tr>
<tr>
<td>modified HBSM</td>
<td>type 1 N IGBTs+</td>
<td>passive</td>
</tr>
<tr>
<td></td>
<td>type 2 N IGBTs+</td>
<td>passive</td>
</tr>
<tr>
<td></td>
<td>type 3 3N diodes</td>
<td>passive</td>
</tr>
</tbody>
</table>

Table 1 Comparison among the improved MMC topologies with DC fault handling capability
The drawback of this scheme, however, is also on high-power losses and device costs, as well as large footprints. For the improved MMC with passive DC FRT capability aforementioned, though the fault current can be forced to zero and DC fault can be isolated from AC side without the external CBs, the converter loses the regulation and support for the AC grid during the fault, which as a result will severely affect the connected AC grid, especially in a weak AC grid.

To solve the above-mentioned issues in the traditional DC FRT schemes, recently, a concept of active DC FRT strategy was proposed [24, 27, 28, 32, 37, 38, 43, 44, 57]. In contrast with the traditional strategies, the active strategies not only have DC fault isolating capability, but also emphasise on the continuous operation of the converter during the fault so as to remain the regulation and support of the AC grid. The factors affecting active DC FRT capability of MMC-based HVDC systems mainly include two aspects: one is type of DC link and the other is the converter topology [49]. Unlike cable faults that are usually permanent fault and must be located and disconnected from DC grids to take repair, temporary DC faults on the overhead lines such as flashovers and voltage dips, which are usually caused by lightning strikes or mechanical faults caused by broken branches or bushes, they can normally be cleared in a short time. Under such conditions, if the converter has the active DC FRT capability, the active FRT scheme can be fulfilled.

In this section, the general active DC FRT operation sequence is summarised, and different active DC FRT strategies based on various improved MMC topologies are presented. As an extension, the control strategies of improved MMC with active DC FRT capability in multi-terminal and hybrid-HVDC systems are also briefly introduced.

5.1 General control sequence of active DC FRT

For active DC FRT operation, the converter is able to continue operating under the reduced DC-link voltage (even $v_{dc} = 0$). This means that the converter can not only block the DC fault, but also continue operating to regulate its output current to the AC side, for example, to support the healthy AC grid and provide fast fault recovery and system restart. The control sequence of HVDC system can be divided into the following three stages, and the relative flowchart is illustrated in Fig. 12 [29].

Stage 1: When a DC fault occurs, the DC-link voltage collapses immediately. Under such a condition, the $d$-axis reference AC current for active power would reduce proportionally, (i.e. when $v_{dc} = 0$, $I_d^* = 0$), while the $q$-axis reference AC current for reactive power can remain unchanged or set to a new value to support the AC grid. For systems using overhead line, automatically system recovery may be required as the DC fault might be temporary. For future large multi-terminal HVDC system using cables, the faulty branch maybe isolated by protection devices, e.g. DCCB and rapid system restart for the healthy network might be required. In this case, the control process moves to Stage 2 for the recovery operation.

Stage 2: A small DC-link reference voltage is provided and the system tries to build up the DC-link voltage. If the DC voltage can be built up successfully indicating the clearance of the DC fault, the control process moves to Stage 3. Otherwise, the DC-link reference voltage sets to zero again and the system waits for the next attempt for rebuilding the DC-link voltage.

Stage 3: The restart process can be considered under an initial condition of $v_{dc} = 0$ in accordance to (8). A ramp signal for the DC voltage reference can then be set and by controlling the $d$ and $q$ axes DC currents the DC-link voltage can be built up smoothly.

5.2 Control strategy of different improved MMC topologies with active DC FRT capability

According to the above analysis, four of all proposed improved MMC topologies given in Table 1 have the active DC FRT capability, and several recently published literatures [25, 28, 29, 33, 38, 44, 45, 58] are related to the active DC FRT methods for MMC. The control strategies of improved MMC with active DC FRT capability or the DCCB, suitable protection strategies are required in order to detect and locate the DC fault quickly and to make sure that only the affected line segment is disconnected selectively by means of the corresponding CB [49]. A ‘handshaking’ method was proposed for the VSC-MTDC systems to locate and isolate the faulted DC line segment [19]. In this method, the changes of magnitude and direction of DC fault currents are used to locate the faulted DC line and then the relative fast DC switches are marked for opening. After the fault currents are extinguished by opening all the ACCBs, the marked DC switches open to disconnect the faulted DC line segment. Finally, the ACCBs close again, the remaining healthy parts of VSC-MTDC systems recover to normal operation. Owing to relatively slow action response of ACCB, the recovery of system is quite slow. To solve

Fig. 12 Flowchart for DC FRT strategy
this issue, FB-MMC was adopted to replace the two-level VSC plus ACCBs to enhance the dynamic response of the MTDC system during DC fault conditions [75], and a three-terminal FB-MMC-based DC grids with DC switches is presented in Fig. 13.

5.4 Improved MMC with active DC FRT capability in hybrid HVDC systems

The conventional line commutated converter (LCC)-based HVDC (LCC-HVDC) systems using thyristor have long been used for bulky power transmission and proven to be superior to VSC systems for high-power rating in terms of cost and reliability [76, 77]. However, LCC systems usually require relatively strong AC systems to operate, and thus become problematic when supplying island networks, e.g. offshore wind farms. In addition, they require larger footprint than VSCs and thus are more difficult for offshore installation. In contrast, VSC-based HVDC system using IGBT is the preferred DC technology for connecting wind farms due to its advantages of independent active and reactive power controls, flexible AC system control and support which are particularly important for offshore wind farms, and more and more VSC-based MTDC systems have also been developed. Following this trend, a large hybrid MTDC system would be developed by adding new VSC and/or LCC converters to existing HVDC networks. For example, there are already significant numbers of LCC-HVDC systems in operation in China and VSC converters connecting newly developed wind farms could be added with their DC sides connected to existing HVDC networks. A classic hybrid HVDC system with a VSC rectifier connecting wind farms and an LCC inverter connecting AC grids is presented in Fig. 14.

DC fault is a not serious issue for LCC-HVDC systems due to their nature of being current source, and detailed analysis on its cause as well as control and protection strategies have been well documented [78]. In the hybrid HVDC system, however, a DC fault can result in serious consequences for the VSCs due to the existence of VSC’s freewheeling diodes [66]. In [79], a hybrid HVDC system comprising an LCC rectifier regulating DC current and an MMC inverter regulating DC voltage with high-power diodes installed in the overhead line was presented. In case of a DC fault, the fault current paths in the MMC inverter are blocked by the high-power diodes.

Except for the common environmental factors or DC line faults resulting in DC faults, a commutation failure in the LCC inverter is also equivalent to a short circuit on the DC side in the hybrid MTDC system. In [80], for the hybrid HVDC system with a VSC rectifier and LCC inverter, the VSC controls the DC voltage and the LCC regulates the DC current. To reduce the probability of commutation failure, a voltage-dependent current limit control is added to the LCC inverter, and the characteristic curve of DC voltage and current in the hybrid-HVDC system is shown in Fig. 15. However, this method has two limitations. First, an extra fast communication between the VSC and LCC which can be expensive and causes for possible failure is needed to request the VSC to reduce DC voltage when disturbance on the LCC AC network is detected. Second, the DC voltage margin for conventional VSCs is fairly small since VSCs need almost constant DC voltage to ensure stable operation. Therefore, the scheme is difficult to realise in real system and is ineffective. Focusing on the above-mentioned issues, in [81], the hybrid MMC topology comprising HBSMs and FBSMs considered for the rectifier at the wind farm side and a maximum DC current controller were proposed. With the advantages of the hybrid MMC on continued
operation at reduced DC voltage, the rectifier at the wind farm side is capable of reducing its DC voltage output to restrain the DC current rise; in the meantime, the hybrid MMC continues regulating its AC network, e.g. providing AC voltage and frequency control for offshore wind farms or regulating the active and reactive powers for grid connected on shore wind farms. A close-loop maximum DC current controller was proposed to limit the DC fault current rise by regulating the DC voltage in the hybrid MMC, as shown in Fig. 16. On the basis of this controller, the DC current can be considered as an indicator between the VSC and the LCC for coordinated control instead of extra communication between the converters.

6 Conclusions

This paper summarised the latest techniques to improve the DC FRT capability of MMC-based HVDC system, in terms of converter topologies and control strategies. The principles of active DC FRT were analysed and then various MMC topologies with DC FRT capability were presented. Besides, a comparison on the extra power semiconductor number and ride-through capability was conducted. Furthermore, utilisation of the improved MMC topologies on HVDC systems was introduced. Focusing on the issue of DC FRT, the latest control strategies, control sequence and protection were presented.

It can be concluded that active DC FRT capability for MMC-based HVDC has been increasingly drawn attention, with the extension of DC grid techniques. In contrast with the concept of passive DC FRT, the active DC FRT capability highlights the continuous operation during the DC fault, so as to regulate and support the connected AC grid, except for isolating the DC fault. Undoubtedly, with the development of DC grids, in particular with overhead lines, DC FRT capability is a prospective technique for the extension of DC grids.

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8 References


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