Review of different fault detection methods and their impact on pre-emptive VSC-HVDC dc protection performance

Bin Chang1,2, Oliver Cwikowski2, Mike Barnes2, Roger Shuttleworth2, Antony Beddard2, Paul Coventry3

1Global Energy Interconnection Research Institute, Future Science Park, Beijing 102209, People's Republic of China
2The University of Manchester, Oxford Road, Manchester M13 9PL, UK
3National Grid, National Grid House, Warwick CV34 6DA, UK
E-mail: changbin_GEIRI@126.com

Abstract: Multi-terminal voltage-sourced converters (VSC) high-voltage direct current (HVDC) transmission system is expected to play a vital role in future power systems. Compared with ac power transmission, dc transmission is more vulnerable to faults due to low dc-side impedances and sensitive power electronics in the converters. Dc protection issues must be tackled before any multi-terminal VSC-HVDC grid can be built. The multi-terminal VSC-HVDC system is studied in detail using switching models for two-level converters, detailed equivalent models for the modular multi-level converters, detailed hybrid circuit breaker switching models and frequency-dependent phase models for dc cables. Using such high-fidelity system models, a systematic study of HVDC fault protection methodologies in more detail than previous studies is conducted. This is the first comprehensive study that includes pre-emptive circuit breaker operation. The results presented in this study underline the benefits of such a detailed treatment of the breaker, and of considering it as part of a fast power electronics system rather than isolated dc equipment. The study identifies the best existing fault detection method and tests it extensively. In order to further improve post-fault system recovery response, which is a key but often neglected part of previous studies, a novel bump-less transfer control has been implemented in the converters.

1 Introduction

Dc transmission will play an important role in future power transmission networks. In Europe, the construction of 12,600 km of dc links is planned in the next decade [1]. Presently, there are two types of technology in the high-voltage direct current (HVDC) transmission arena: current-sourced converters (CSC) and voltage-sourced converters (VSC). As discussed in [2], VSC-HVDC offers several advantages over CSC-HVDC particularly for offshore applications, such as compactness, and flexible control of active and reactive power etc. VSC-HVDC is a more practical solution for transmitting offshore electrical energy to land, in the condition that the power transmission distance is >60–100 km [3–5].

For the meshed dc transmission, protection is an essential area of study, since due to low dc-side impedance, the fault current will rise to a high value within a very short period of time. To limit the impact of faults, a fast and reliable protection system is required. Some VSC topologies are capable of controlling dc-side fault currents, but the technology has not so far been deployed in power transmission networks. Traditional protection methods employed in ac systems, like impedance relays, are not applicable for VSC dc protection [6, 7]. Leterme and VanHertem [8] have proposed dc protection requirements, along with some protection operation strategies, such as open-grid and grid-splitting protection strategies. However, there is no standard method for dc protection operation at present.

Various methods have been proposed for fault detection; overcurrent, derivative and waveform protection have all received attention [7, 9–12]. In [13], a detection method based on travelling waves was proposed. In [7], the fast dyadic waveform transform method was proposed; however, in this scheme large amounts of data must be processed potentially resulting in long delays. In [14], voltage derivative methods were used for dc fault detection; however, as shown in Section 3, this method is very sensitive to noise.

Grounding configurations will influence the dc protection system design. Bucher and Franck [15] highlight the impact different grounding schemes exert on dc fault current. Based on [15], a solid earthing (low impedance grounding) will result in the system experiencing high fault currents, but the overvoltage level of the system will be low. If the system’s grounding impedance is high, during the dc-side fault, a high overvoltage will be expected for the system and the system’s fault current level is low. In terms of the influence of the grounding location, Bucher and Franck [15] point out that if the grounding is only conducted at a single terminal rather than all dc terminals, the performance of the overvoltages in such a system will be worse. Leterme et al. [16] also discuss the influence of the grounding location on the design and protection of the dc system: the grounding location will exert a significant impact on the system’s pole-to-ground fault response and the earth current during system’s normal operation. Based on [16], if the HVDC grid is configured as the asymmetric monopole, only low impedance grounding could be adopted and the grounding point is at one end of the converter. Under such a configuration, if a pole-to-ground fault occurs, the fault current will increase to a high value within a short period of time, which means fast and reliable fault detection and isolation methods are required under such HVDC scheme. For the symmetric monopolar HVDC system, a neutral point is available for each converter in the dc system. If this neutral point is grounded by a high impedance, the system will experience high overvoltage during a dc-side fault. Here in this paper, a low-impedance grounding configuration is used since this results in less severe requirements for the dc cable [17].

In this paper, different protection systems have been studied in a high-fidelity four-terminal VSC-HVDC system model. The proactive hybrid circuit breaker developed by ABB is used to perform fault isolation and is modelled in detail. Based on a study of different dc fault detection methods, waveform transform methods have been found to be promising and capable of discriminating between other system transients. The continuous wavelet transform (CWT) has been implemented, as shorter computation times can be achieved compared with previous methods [7]. Using the wavelet transform, this paper carries out a systematic study of the transients a dc fault detection system may be exposed to, and includes a range of non-fault transients, dc.
faults and post-fault transients. As part of the protection system design a novel bump-less transfer control is proposed to improve the dc system's post-fault recovery response.

For the first time, the impact pre-emptive control has on the overall protection system has been studied.

2 System description and modelling

The four-terminal VSC-HVDC system modelled, shown in Fig. 1, has a combination of two-level and modular multi-level converters (MMC). Currently in the VSC-HVDC industry, the trend is to employ more MMC; but many of the commissioned VSC-HVDC projects are based on two-level converters, for example the BorWin1 and Estlink projects [18]. Therefore, it is possible that future multi-terminal dc grids will be based on a combination of two-level and MMC, and possible interactions should be considered. In the VSC-HVDC system shown in Fig. 1, the system operates at ±300 kV. The grounding configuration of this multi-terminal system is based on Borwin1 [19], which grounds the mid-points of all the two-level converters. Note the resistances connected to the grounding points are parasitic resistances.

2.1 Hybrid dc circuit breaker modelling

The proactive ABB hybrid circuit breaker contains a load commutation switch (LCS) in series with an ultra-fast disconnector (UFD) and a main breaking element based on IGBTs. The operation principle of the hybrid circuit breaker is well documented in [20, 21]. Based on [22], a parasitic inductance of 30 μH has been added to both the LCS and main breaker branches. Table 1 shows the values of inductors, capacitors and varistors used in the hybrid circuit breaker model.

Breaker actions coincide with fault sensing – coordinating and interaction of these events is thus important. By using the detailed hybrid circuit breaker model, the impact of the pre-emptive operation method (discussed in Section 4) on the system fault response can be examined. The detailed model gives a more accurate estimate of the protection operation speed.

2.2 Other VSC-HVDC system component modelling

The two-level converters are modelled with switched IGBTs, phase reactors, transformers and dc-link capacitors. Various control methods have been developed for the VSC-HVDC multi-terminal system, such as voltage margin control, voltage droop control etc. [23, 24]. The onshore two-level model here employs voltage droop control [25]. The offshore converter is controlled to directly provide the offshore ac grid voltage and frequency [26]. In Fig. 1, an aggregated model of the windfarm consisting of 40 wind turbines of 5 MW rated power is used. The wind turbine back-to-back converter is modelled with an averaged model, and the offshore side transformer configuration is based on [27]. Dc choppers have been employed in each onshore converter's dc terminal to regulate dc-link voltage [28] and are detailed in Table 2.

In terms of MMC modelling, different types of MMC model have been developed in [29–31]. The MMC model employed in this paper uses the detailed equivalent model (DEM). The reason for choosing the DEM is that based on [31], it can virtually provide an identical system response to the TDM, but takes significantly less time to run. Compared with DEM, the AM is more limited in its application [31]. In the DEM used here, there are 30 sub-modules in each phase arm which provide 31 voltage levels. The MMC station in this paper is configured to control active and reactive power.

Cable modelling is of great importance for conducting dc protection, as the cable model will have a significant impact on how cable voltage and current vary during simulations. Based on [32], the FDPM is the most accurate time-domain line model and was therefore chosen to be employed in this paper.

3 dc detection method comparison

The aim of this section is to determine the best method for detecting dc faults. This aim is achieved by analysing different
detection methods and simulating them to evaluate their performance.

This paper assumes that each dc circuit breaker will require a high-value inductance to limit the peak fault current it is exposed to. Many proposed dc circuit breaker designs require a high-value series inductance [20, 21, 33, 34].

For each simulation, the initial system conditions are: the dc-link voltage is 585 kV, current flowing from converter stations A to B, I_{ab} is 1.2 kA, I_{ac} is 0.57 kA, I_{cb} is 0.88 kA and I_{db} is 0.025 kA. In steady state, the offshore windfarm, connected to station C, is sending 200 MW power to the HVDC system. Converter station A sends 1000 MW to the HVDC system. Converter stations B and D receive 700 and 500 MW, respectively.

Each of the following protection methods is evaluated in the four-terminal system as shown in Fig. 1. For each case, a 0.01 Ω pole-to-pole fault is applied 20 km away from station A on the line between stations A and B, at 3 s.

3.1 Overcurrent protection

Overcurrent protection for VSC-HVDC system has been studied in [35]. The problem with overcurrent protection is that, in order to achieve desired fault discrimination, overcurrent protection requires a high-current threshold value and so it will take a relatively long time for the dc breaker to reach the fully open position. Further, if there is a high impedance fault occurring in the dc system, it is highly likely that this fault may not be detected since the fault current in this case may not exceed the threshold value.

Fig. 2a shows the current at converter stations A, C and D when a fault is introduced. As can be seen from Fig. 2a, when the fault occurs, I_{ab}, I_{ac} and I_{db} start to increase. When the current I_{ab} reaches the overcurrent threshold value, the corresponding circuit breaker starts to isolate the fault. During operation of the circuit breaker, currents I_{ca} and I_{db} continue to increase. Therefore, in order to obtain good fault discrimination and prevent circuit breakers mistripping, the overcurrent threshold value should be set at a high value, and this threshold value is dependent on the isolation speed of the circuit breaker. In this case, the threshold value is set at 3.2 kA. There is clearly a trade-off since a high threshold delays the breaker's operation and results in higher fault currents. Based on [6], overcurrent protection may be employed as backup protection. It will not be considered any further in this paper.

3.2 Current differential protection

Current differential protection is often employed in ac systems protection, and the fault protection algorithm is simple and easy to implement [36]. The method has problems though if used for dc: the cable's capacitive current may cause mal-operation of the circuit breakers during voltage transients. In addition, as the direction of current at each dc terminal is compared in this algorithm, fast communications between each converter station are required to avoid long delay in fault detection. It should be noted that, when a pole-to-ground or pole-to-pole fault occurs, the fibre-optic cable used to communicate between converter stations may also be damaged. Consequently, the shortest communication route between converters can no longer be taken. A longer route via other healthy cable sections must be taken instead, introducing a longer time delay in fault detection (if indeed such a route exists).

Referring to Fig. 1, under normal conditions, I_1 + I_2 should be approximately zero. When a dc fault occurs I_1 + I_2 will be non-zero, indicating a dc fault. Fig. 2b shows simulation results using current differential protection, when a pole-to-pole fault is introduced. The communication delay time here is 1.1 ms, and assumes the signal has to travel via other converter stations (A → C → D → B, i.e. 220 km). Due to the communication delay, differential protection cannot detect the fault within a short period of time. Differential protection may be employed, however, to detect high impedance faults, as a supplementary fault detection system.

![Fig. 2 System response based on different protection methods](image-url)
3.3 Under voltage protection

Under voltage protection previously has been applied in ac system [37]. The voltage drop, which is caused by the fault in the system, can be measured and compared with corresponding threshold values to perform fault detection. However, in the event of a dc fault, the voltage across all converter terminals will drop and therefore proper discrimination cannot be achieved. Figs. 6a and b show an example of this drop which can be seen to occur just after fault application.

3.4 Voltage derivative protection

Voltage derivative protection has been proposed as a primary protection method [9]. When a dc fault occurs in the four-terminal VSC-HVDC system, terminals that are closer to the fault will have a higher voltage derivative, than those far away. Therefore, the values of voltage derivative can be used to detect and locate the dc fault. Differentiating the signals, however, makes the method sensitive to noise.

Fig. 3a shows the voltage across converter station B, when a high impedance pole-to-ground fault (e.g. 100 Ω) occurs at 3 s between converter stations A and B. When the voltage signal is measured and down-scaled to feed into a microcontroller for signal processing, noise is introduced, resulting in the voltage signal being distorted, as shown in Fig. 3b. Figs. 4a and b show the results of the voltage derivative method for the signal without and with noise. It can be seen from these two graphs that, when noise is introduced, the voltage derivative method fails to discriminate between the fault condition and normal operation.

3.5 CWT protection

The protection needs to be implemented in real time, thus only a small amount of sampled data should be used to detect a fault in order to limit computational delays. Wavelet detection is well suited to such a scenario.

The continuous wavelet coefficient of a given signal \( f(t) \) can be calculated using (1), where \( a \) is the scale or window size and \( b \) is the position:

\[
\text{CWT} = \int_{-\infty}^{\infty} f(t) \cdot \Psi_{a,b}(t) \, dt \quad (1)
\]

where

\[
\Psi_{a,b}(t) = \frac{1}{\sqrt{a}} \Psi \left( \frac{t-b}{a} \right)
\]

Given the Fourier transform of the selected mother wavelet, the Fourier transform is applied to the signals to be processed. These results are multiplied and the inverse Fourier transform is applied to obtain the CWT coefficients. Based on [10], the Haar wavelet is capable of giving the sharpest edge compared with other mother wavelet types and is used here

\[
F(\text{CWT}) = je^{-j\omega t/2} \sin(\omega t/4) \sin(\omega t/4) / (\omega t/4)
\]

Based on Euler’s theory, the Fourier transform of Haar wavelet can be transformed into

\[
Z = e^{-j\omega t/4} \left[ \cos(\omega t/2) - j \sin(\omega t/2) \right] \left[ \sin(\omega t/4) / (\omega t/4) \right]
\]

In this application, the signals to be processed are discrete time series data, hence the Fourier transform of the signals to be processed is

\[
X_k = \sum_{n=0}^{N-1} x_n e^{-2\pi jkn/N} \quad (4)
\]

By comparing the wavelet coefficients generated from the calculations with a threshold value, the fault can then be detected. Fig. 3c shows the CWT (scale \( a = 15 \)) coefficients obtained from the signals as shown in Fig. 3a. It can be seen from Fig. 3c that when no measurement noise is considered, during normal operation, the CWT calculation produces a low value coefficient. When a fault occurs, the CWT provides a high coefficient due to faster transients that appear on the system. This change can be used to detect the presence of a fault. This requires a threshold value to be determined as other system transients and noise will increase the coefficient generated by the CWT calculation. Fig. 3d shows an example case when noise is added to the measured signals, showing that the coefficients generated during normal operation are non-zero.

3.6 Discrete wavelet transform (DWT) protection

The DWT takes the form

\[
\text{WT}(u, 2^j) = \int_{-\infty}^{\infty} f(t) \frac{1}{\sqrt{2^j}} \Psi \left( \frac{t-u2^j}{2^j} \right) \, dt \quad (5)
\]
There are fast wavelet calculation algorithms available, e.g. the Mallat Tree Algorithm, which can speed up data processing [38]. In this algorithm, the signals to be analysed are passed to two separate filters – low pass and high pass. The Haar wavelet is chosen as the mother wavelet and at each level the coefficients obtained from the low-pass filter are

\[ A_i = \frac{1}{2} \sum_{m=1}^{N} c_{i-m} f_m, \quad i = 1, \ldots, N/2 \quad (6) \]

The coefficients obtained from the high-pass filter are:

\[ D_i = \sqrt{2} \sum_{m=1}^{N} (-1)^{m+1} c_{i+m} f_m, \quad i = 1, \ldots, N/2 \quad (7) \]

In (6) and (7), \( f \) is the input signal, \( c \) is the Haar wavelet coefficients, where \( c_0 = c_1 = 1 \) and \( \forall c_m = 0 \) if \( m \in (-\infty, 0) U [2, +\infty) \). The multiplication by \( \sqrt{2} \) in (6) and (7) is needed to enable the Haar transform to preserve the signal energy. In this paper, the level of DWT for both voltage and current signals is chosen to be 4. Figs. 4a and b show the DWT-based protection system response.

The scale or level one chooses for the CWT and DWT calculation impacts the change seen in generated coefficients, which provides the means of fault detection. Fig. 4a shows a comparison of the fault signals generated by CWT, DWT and voltage derivative detection methods, indicating that any of these methods are feasible in very low-noise environments. However, as can be seen in Fig. 4b, CWT with a scale of 20 gives a higher change of coefficient than the scale of 5. However, using a higher scale requires more data to be processed, which in turn makes the method computationally intensive. As a compromise between protection system performance and data processing speed, the CWT scale used here is 15. The voltage and current signals are sampled at a frequency of 10 kHz. By choosing an appropriate threshold value (e.g. 0.9), the fault can be detected even when a noise signal is introduced, see Fig. 4b.

4 Pre-emptive protection

Hybrid dc circuit breakers are capable of being operated in several different ways once incipient faults are detected. Due to their multi-staged operation, new operational techniques are being developed to better exploit their designs. Concepts such as serial operation, open-grid and pre-emptive operation are examples [8, 20]. In order to reduce the time it takes to isolate the fault as well as to make full use of the hybrid circuit breaker, a pre-emptive operation method is proposed in [20].

This method prematurely commutates the current flowing through the UFD to the main breaker once the current has exceeded a 'pre-emptive' threshold value, prior to the fault being confirmed and that a given circuit breaker should open. This is done in all breakers that experience a current exceeding the pre-emptive current threshold. Pre-emptive operation allows part of the circuit breaker's operation to occur in parallel with fault detection. Once the fault is confirmed, the UFD is opened and afterwards the main breaker will be switched off. If there is no fault, the LCS will be reclosed and current flow returned to the main path. The pre-emptive method involves opening all UFDs in the circuit breakers that will be required to provide primary and backup protection. Pre-emptive operation allows backup protection to be provided very rapidly.
5 Wavelet fault detection study

This section conducts a fault detection study using CWT, which has been identified as a promising method in the previous section, and has not been extensively studied in previous VSC-HVDC protection literature. The structure of the fault detection system is modified from [7]. Fig. 5a shows that two of three signals are required to confirm a fault. Fig. 5b shows the locations of each measured signal for the positive pole. The threshold value used to detect the fault was determined through a sensitivity study for the four-terminal system. Note that sensor delays are included. Based on [39, 40], the voltage measurement delay \( T_1 \) is around 33 ms and the current measurement delay \( T_2 \) is around 40 ms.

The proposed CWT detection method has been examined under different transient scenarios to ensure each breaker has proper discrimination. Each transient event occurs at 3 s. For each case, the maximum CWT coefficient across all dc terminals is plotted. A signal-to-noise ratio (SNR) of 30 dB is considered in this paper.

5.1 ac-side solid three phase to ground fault

When there is an ac-side fault, the dc detection system should not respond. Fig. 5c, scenario A, shows the dc detection system's response when a three-phase to ground fault occurs at the point of common coupling of converter station A. If any converter station blocks, the dc detection system should not respond. Fig. 5c, scenario B, shows the dc detection system's response when converter station A blocks. The CWT coefficients for voltage and current signals are smaller than the threshold value; therefore, the dc detection system will not trip the circuit breaker.

5.3 VSC-HVDC system emergency power flow reversal

Another scenario to test is when the VSC-HVDC system has to provide emergency power flow reversal. Fig. 5c, scenario C, shows the dc detection system does not respond when converter station D reverses its power flow at 3 s. The power flow reversal rate is 1 GW/s.
5.4 dc-side high impedance pole-to-ground fault

This section examines the dc detection system’s response to a high impedance pole-to-ground fault (e.g. 100 Ω). Fig. 5c, scenario D, shows the dc protection system responds when a high impedance fault occurs.

5.5 dc-side low impedance pole-to-pole fault

When a pole-to-pole fault is introduced to the four-terminal system the detection system should respond. A 0.01 Ω pole-to-pole fault was introduced between converter stations A and B and the fault is 20 km away from converter station A. From Fig. 5c, it can be seen that the protection system detects the fault.

Figs. 6 and 7 show all the dc fault detection systems’ responses under scenario E. A measurement noise of 30 dB is applied here to show the wavelet method can reject the noise.

As can be seen from Fig. 6a, in the event of a pole-to-pole fault occurring between converter stations A and B, the voltages across the dc-link collapse to zero. At the same time, I1 and I2 increase to a high value, as shown in Fig. 6c. The terminal voltages for the other links are shown superimposed in Fig. 6b, and the other branch currents are shown superimposed in Fig. 6d. The wavelet method can correctly discriminate between faults. This is shown, since only the wavelet coefficients of the dc link between stations A and B exceed the threshold value, Figs. 7a and c. For non-faulted cables, the wavelet coefficients stay below the threshold value, Figs. 7b and d.

6 Bump-less transfer control

As shown by the previous section, dc fault detection can be provided by wavelet methods. However, even with fast fault detection and isolation the dc voltage is still significantly disturbed after the fault is cleared, Fig. 8a. Knowing how the converter responds after fault isolation is an important part of any dc protection system design, as the power system equipment must be able to deal with the lingering effects that dc faults impose on the system.

Based on [41], the dc overshoot ripple voltage should be within 5% of the rated dc voltage; high-voltage ripple may damage dc-side components or require devices of a higher voltage rating. To reduce the over-voltages seen in Fig. 8a, a bump-less transfer controller is proposed [42], Fig. 8b. Based on the system recovery method proposed in this paper, when the fault is confirmed, the converter will block. After a certain amount of time (e.g. 100 ms), the converter will un-block and a low bandwidth controller is used.
initially so the terminal voltage increases slowly to reduce any voltage overshoot in the dc system, and reduce potential voltage oscillations at converter terminals. A high bandwidth controller is then used once the system has reached normal operation.

A comparison of the original control strategy and the bump-less control strategy is shown in Fig. 8, indicating that the modified control strategy can provide a significant peak voltage reduction.

7 Protection system study

All dc protection systems will consist of a fault detection method, circuit breaker operation philosophy and a converter control strategy. Each of these is a key element and any protection strategy should consider all of these. The protection study performed in Section 5 has shown that wavelet detection methods can provide a robust dc fault detection method. Pre-emptive operation of the dc circuit breaker is discussed as a potential circuit breaker operation method in Section 4. Section 6 has shown that bump-less control is beneficial in reducing the peak voltage seen at the converters’ terminals.

In order to compare different potential dc protection systems, a study was performed using a variety of detection methods, circuit breaker operation philosophies and converter control strategies. This study aims to highlight the benefits that can be gained from using the pre-emptive circuit breaker method and post-fault recovery scheme.

Table 3 provides a summary of the protection system comparison study. In Table 3, the semiconductor means the purely solid-state circuit breaker. There are three categories of circuit breaker used: a hybrid circuit breaker, a hybrid circuit breaker using a pre-emptive algorithm and, for comparison, a purely solid-state circuit breaker (semiconductor) (which would be the fastest option but is presently unfeasibly expensive). It can be seen from Table 3 that the implemented CWT method is faster than the DWT method in detecting the fault. However, the fault isolating time is reduced by 1.21 ms (~32%) when the DWT method is used with pre-emptive operation method. Selection of the signal to initiate the pre-emptive operation is key in determining the amount of time saved when using the pre-emptive method, as well as the threshold value that is chosen to start the pre-emptive operation. When a wavelet detection method is used, the circuit breaker’s operation time dominates the protection systems total fault clearing time. For hybrid circuit breakers this is still heavily dominated by the opening time of the UFD. Turn-off the semiconductor branch only takes 250 µs [20]. The post-fault recovery scheme can provide a significant reduction in peak voltage, which is within 2% of the idealised case when semiconductor circuit breakers are used.

8 Conclusions

Dc protection is a technology barrier for the establishment of any multi-terminal VSC-HVDC grid. This paper conducts a detailed study of different protection strategies using a much higher fidelity model than previous studies. Based on the review of different detection methodologies, it is found that wavelet transforms seem to be presently the best option for dc fault detection. Wavelet transforms were then extensively tested for key relevant dc faults and different transient scenarios.

Pre-emptive operation of dc circuit breakers has been implemented to show its impact on the protection operation times. The post-fault converter control strategy has been studied and a method is given to reduce the peak voltages seen by the converters.

A dc protection system study was lastly performed showing the combined effects of three major components; dc fault detection, circuit breaker operation and post-fault converter control. The main findings are:

Table 3 System response comparison by using different protection methods

<table>
<thead>
<tr>
<th>Protection method</th>
<th>Fault isolation time, ms</th>
<th>Peak voltage, kV</th>
<th>Peak current, kA</th>
</tr>
</thead>
<tbody>
<tr>
<td>DWT</td>
<td>3.80</td>
<td>714</td>
<td>10.49</td>
</tr>
<tr>
<td>DWT^3</td>
<td>3.80</td>
<td>655</td>
<td>10.49</td>
</tr>
<tr>
<td>DWT + pre-emptive(^a)</td>
<td>2.59</td>
<td>610</td>
<td>7.94</td>
</tr>
<tr>
<td>CWT</td>
<td>2.60</td>
<td>650</td>
<td>8.00</td>
</tr>
<tr>
<td>CWT^3</td>
<td>2.60</td>
<td>610</td>
<td>8.00</td>
</tr>
<tr>
<td>CWT + pre-emptive(^a)</td>
<td>2.59</td>
<td>610</td>
<td>7.95</td>
</tr>
<tr>
<td>CWT + semiconductor</td>
<td>0.55</td>
<td>615</td>
<td>2.49</td>
</tr>
<tr>
<td>CWT + semiconductor(^a)</td>
<td>0.55</td>
<td>602</td>
<td>2.49</td>
</tr>
</tbody>
</table>

\(^a\)Bump-less control has been used.
(i) For on-line dc fault detection, due to the small amount of data being processed each time, it is feasible to apply CWT and its detections times are shorter compared with overcurrent detection and current differential detection.

(ii) For the wavelet transform, there is a trade-off between protection speed and noise rejection ability.

(iii) For wavelet protection, the fault detection and location are combined in one signal. For pre-emptively operated systems, an additional signal must be used to initiate the LCS. Selection of this additional signal is essential in determining the reduction in time achieved.

(iv) The operational speed of the dc circuit breaker is the dominant factor in fault isolation time.

(v) In order to prove the robustness of the system, the protection factor in fault isolation time.

(vi) Bump-less control can reduce the fault recovery voltage influence the current CWT coefficients.

(vii) Additional care should be given to system power flow as this will determine the magnitude of the current, which in turn will influence the current CWT coefficients.

9 Acknowledgment

The authors gratefully acknowledge the support of National Grid project TAO/22360.

10 References


